REMARKS

Reconsideration of this application is respectfully requested. Claims 1-27 remain pending.

Rejection Under 35 U.S.C. § 112

Claims 1-27 have been rejected under 35 USC § 112, first paragraph, on the ground that the phrase "first signal path that is permanently terminated at the interface device," recited in both independent claims 1 and 17, and the limitation of "a signal path that is permanently terminated at the interface device" recited in independent claim 23 were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully disagrees, and submits that the specification and drawing clearly support a signal path that is permanently terminated at the interface device under § 112, first paragraph. For example, the specification describes an embodiment of a point-to-point high speed signal path which at both, or either end, is isolated from an I/O interface device, having termination circuitry that *remains fixed* to an intermediate interface.[1] A more specific embodiment of such a high speed connection having termination circuitry that remains fixed to an intermediate interface is shown in App. Figure 14. Resistive terminations elements "R" are coupled, without any intervening switching structure, to output nodes of the interface device, and thus, to the signal path, which shows resistive termination elements coupled, without any intervening

[1] "By this arrangement, the high-speed channel 52 and its *active or passive termination circuitry* (which may be located within or external to the integrated circuit device and at both or either ends of the high-speed channel 52) is isolated from the I/O interface 55 contained within the memory elements 56a-56c, effectively segmenting the overall signal path between memory controller 50 and memory elements 56 into two, different-performance channels 52, 54 and *intermediate interface 53*. . . . Also, the high-speed point-to-point channel 52, and its terminating interfaces 51, 53 can be optimized for very high speed operation in a cost-effective manner since *this point-to-point connection remains fixed* as part of the memory system, *in contrast to the memory devices 56 which may be inserted and removed* as necessary to achieve a desired storage capacity." (Paragraphs 0012 and 0013).

switching structure, to output nodes of an interface device and thus to the signal lines that constitute the signal path.[2] Applicant respectfully submits that these statements and figures clearly describe a permanent termination, in contrast to the switched termination structure disclosed in the Greff reference. (See Greff, Fig. 1, element 38).

Applicant submits that this description and "permanently terminated" as used in the independent claims cited by the Examiner falls within the spirit and scope of the terms used in the detailed description as illustrated above, and respectfully points out that the claim language does not need to track, verbatim, the language in the specification. (MPEP 2163).

Accordingly, applicant submits that "an interface device coupled to the memory controller via a first signal path that is permanently terminated at the interface device" as recited in claim 1, and similar recitations in independent claims 17 and 23, are fully and unambiguously supported within the specification and Figures in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. If the Examiner disagrees with the above analysis after examining the cited figures and paragraphs, Applicant respectfully requests a phone call to discuss this matter.

Rejection Under 35 U.S.C. § 103

Claims 1-27 have been rejected under 35 USC 103(a) as unpatentable over U.S. Patent Publication 2002/0083255 to Greff et al. ("Greff") in view of Applicant's Background.

[2] Within the specification, the description of Figure 14A recites, in part, "Figure 14A, for example, illustrates a CML driver 330 that may be used to implement such differential output drivers. The CML driver 330 includes transistors 331 and 333 having drains coupled to respective termination elements (depicted as resistors, R, in Figure 14A, though active load elements may be used) and that form differential output nodes 332 (Tx+) and 334 (Tx-)." (Application, Paragraph 0021).

Claim 1 recites the element of:

"an interface device coupled to the memory controller via a first signal path that is permanently terminated at the interface device"

The Office Action acknowledges that Greff does not disclose or suggest the limitation of a first signal path that is permanently terminated at the interface device, and Applicant submits that Applicant's Background does not teach this limitation either. Specifically, Applicant respectfully points out that the Applicant's Background does not describe any interface device at all. Accordingly, even if Greff and the Background of the Invention could be combined in a manner suggested by the examiner, their combination would still lack the above recited element, and therefore, would not establish a prima facie case for obviousness. For at least these reasons, Applicant submits that the independent claim 1, and claims 2-16, which depend therefrom, and further limit claim 1, stand allowable over the cited art.

Claim 17 recites the element of:

"transmitting multiplexed data from a memory controller to an interface device at a first data rate via a signal path that is permanently terminated at the interface device;"

Applicant submits that, for at least the reasons stated in conjunction with independent claim 1, even if Greff and the Applicant's Background could somehow be combined in a manner suggested by the Examiner, their combination would still lack the above recited limitation, and therefore, would not establish a prima facie case for obviousness. For at least these reasons, Applicant submits that the independent claim 17, and claims 18-22, which depend therefrom, and further limit claim 17, stand allowable over the cited art.

Claim 23 recites, in part,

"a first input/output (I/O) port to receive multiplexed data from a memory controller at a first signaling rate via a signal path that is permanently terminated at the interface device."

Applicant submits that, for at least the reasons stated in conjunction with independent claim 1, even if Greff and the Applicant's Background could somehow be combined in a manner suggested by the Examiner, their combination would still lack the above recited limitation, and therefore, would not establish a prima facie case for obviousness. For at least these reasons, Applicant submits that the independent claim 23, and claims 24-27, which depend therefrom, and further limit claim 23, stand allowable over the cited art.

Conclusion

Applicant submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Authorization is hereby given to charge deposit account 50-1914 for any fee deficiency associated with this Response.

Respectfully submitted
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By: _____

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